FIG. 1

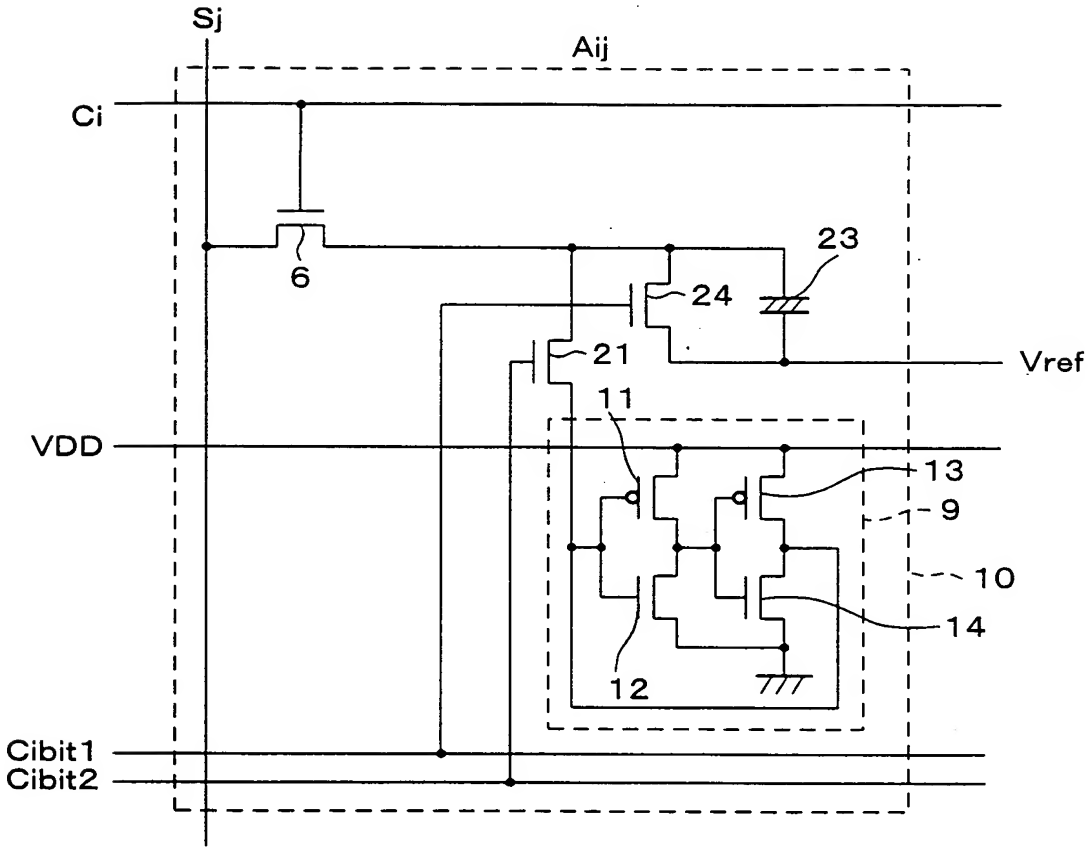

FIG. 2

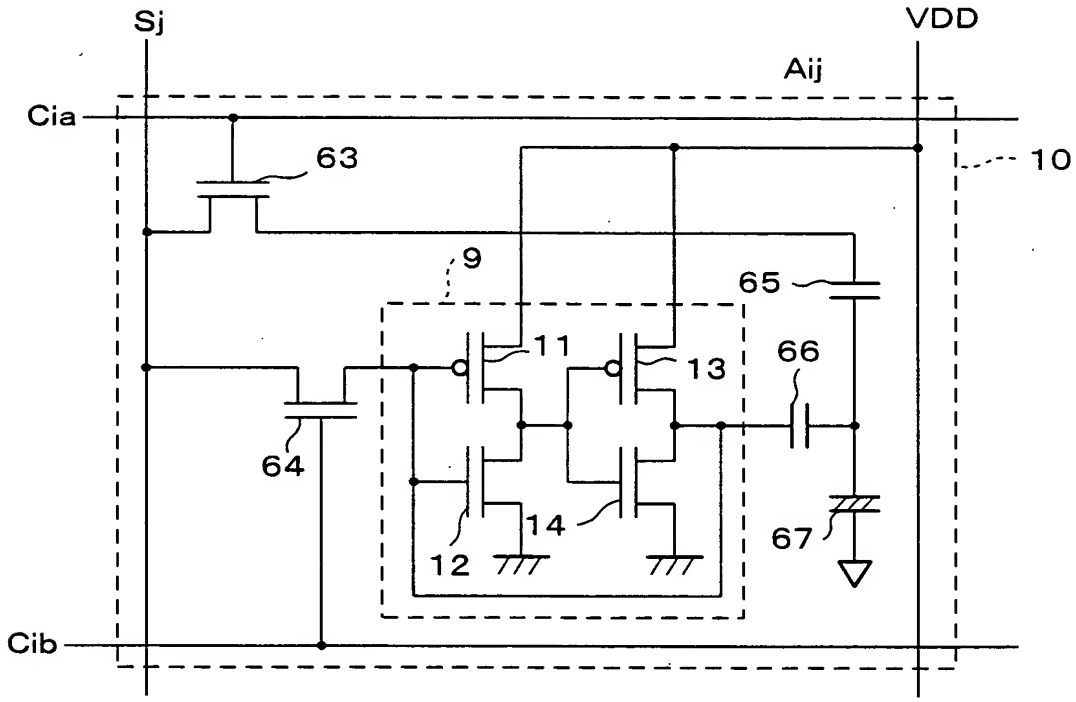

FIG. 3

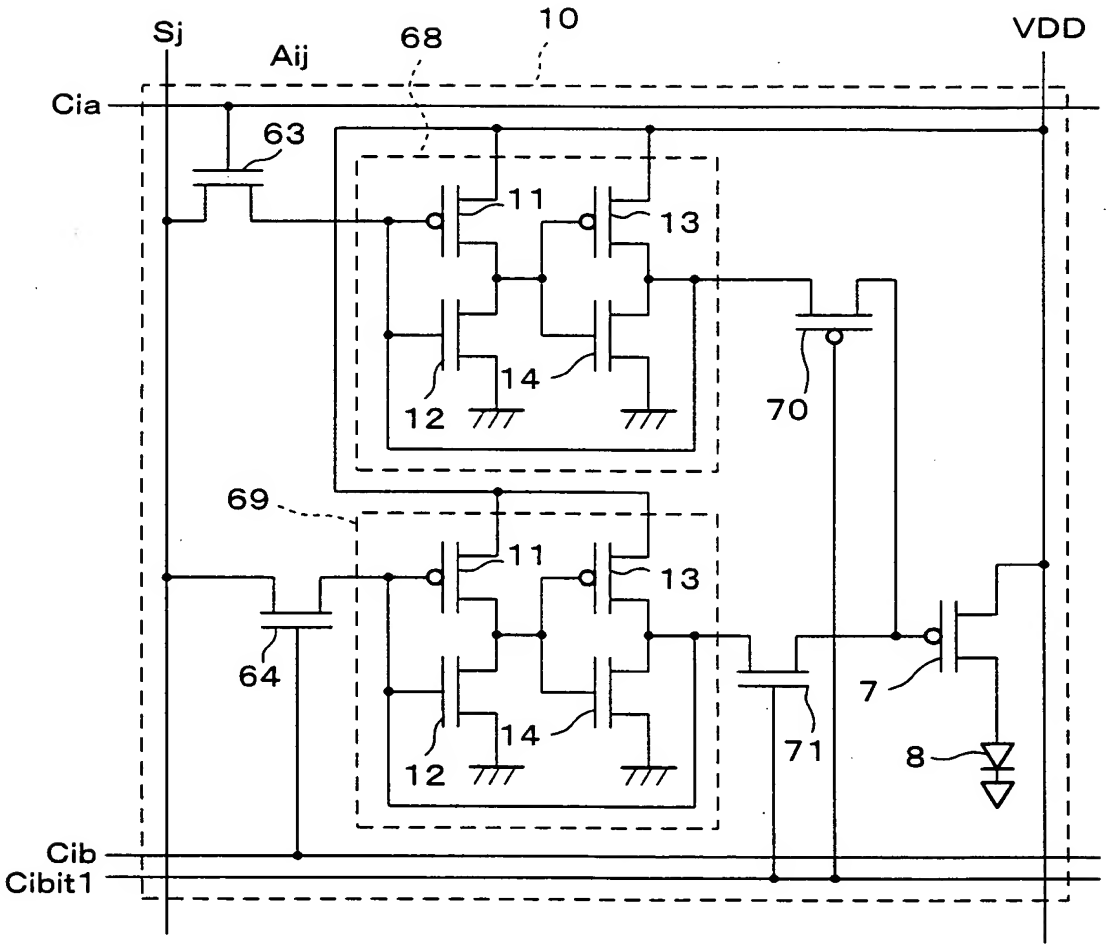
Sj
Aij
68
10
VDD
Cia
63
11
13
14
12
70
69
11
13
64
14
12
7
71
8
Cib
Cibit1

FIG. 4

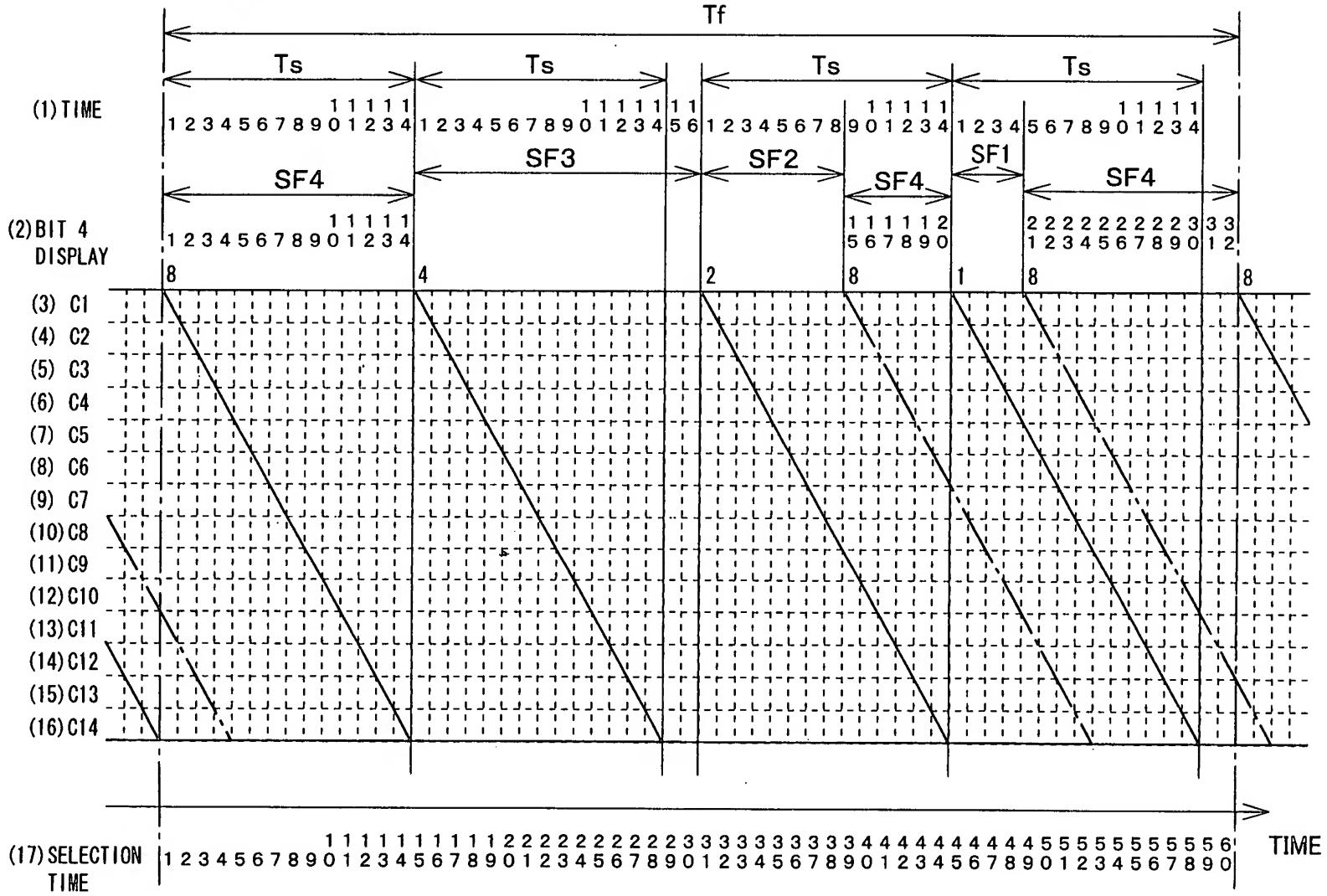

FIG. 5

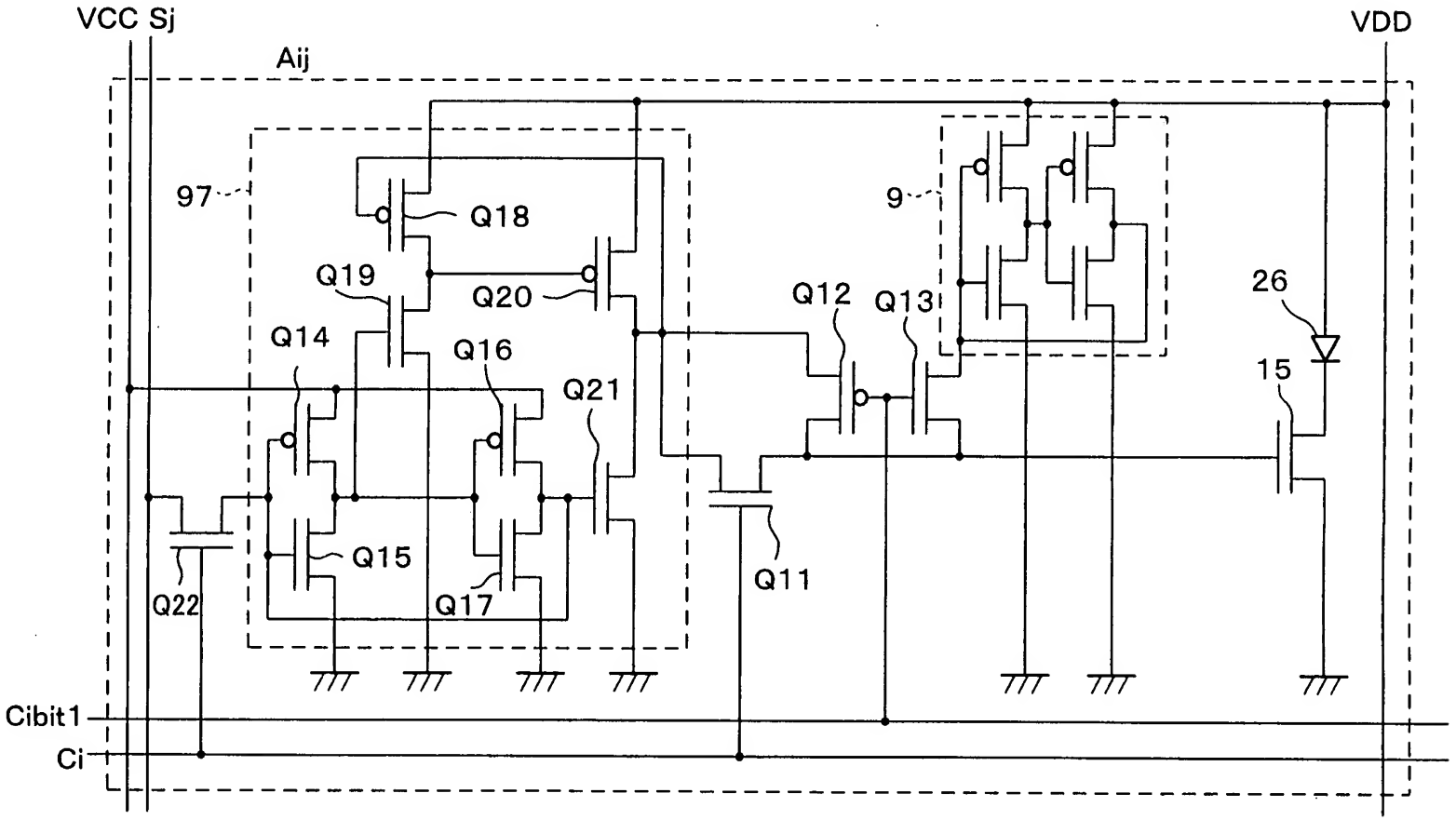

FIG. 6

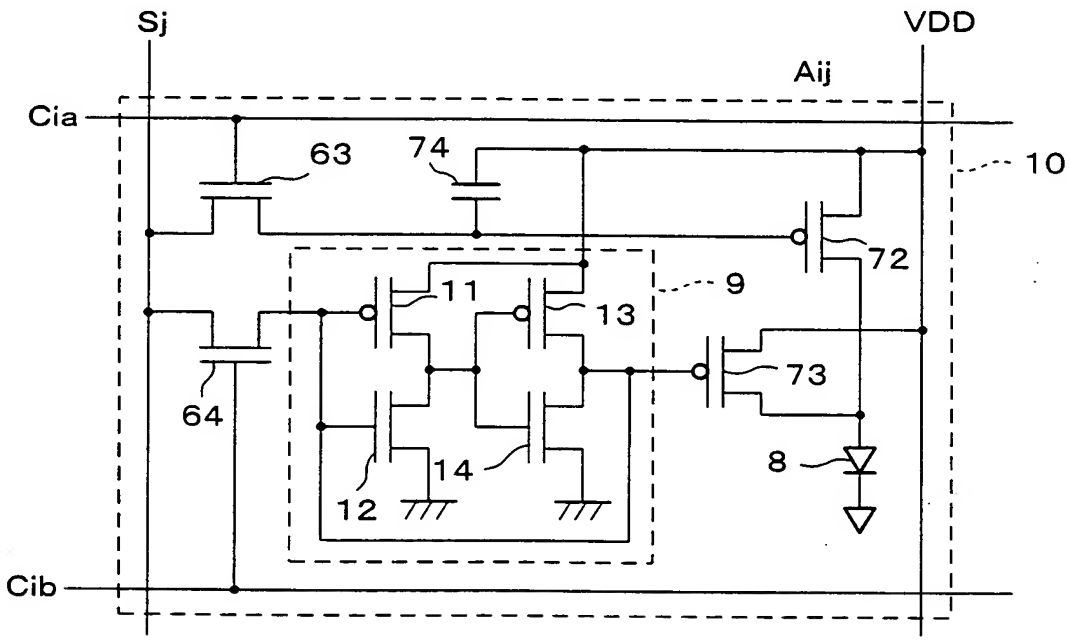

FIG. 7

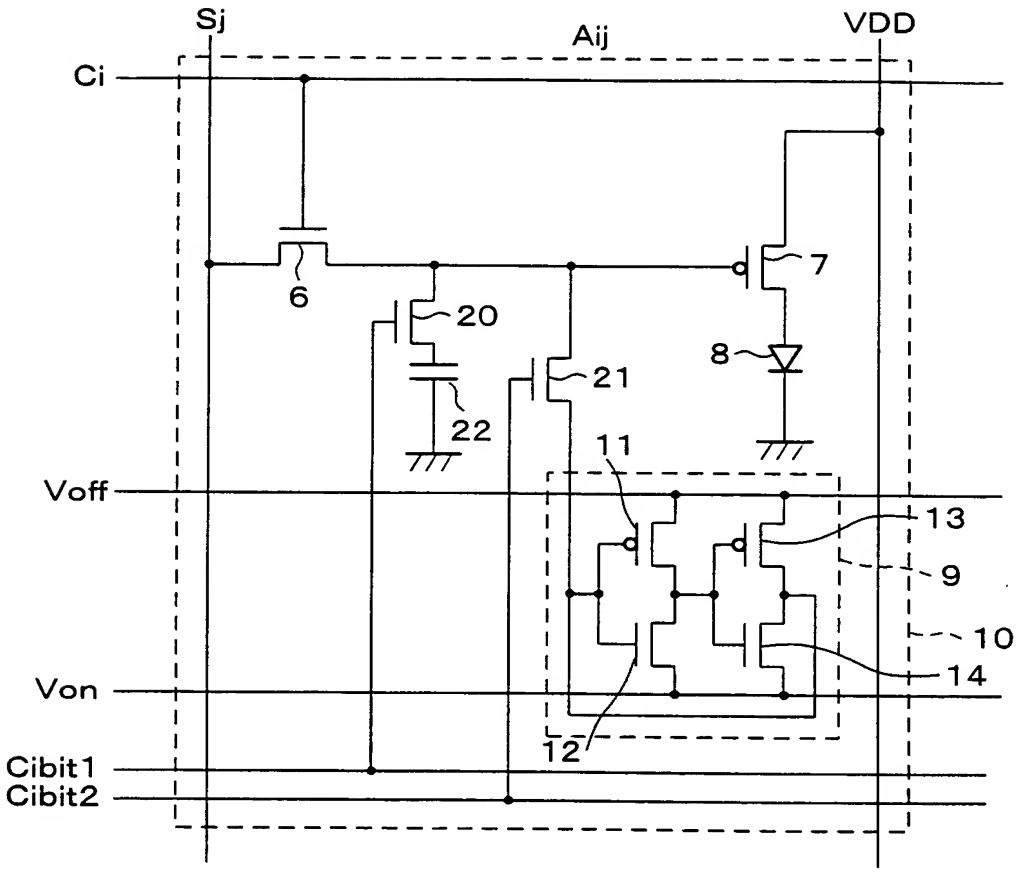

FIG. 8

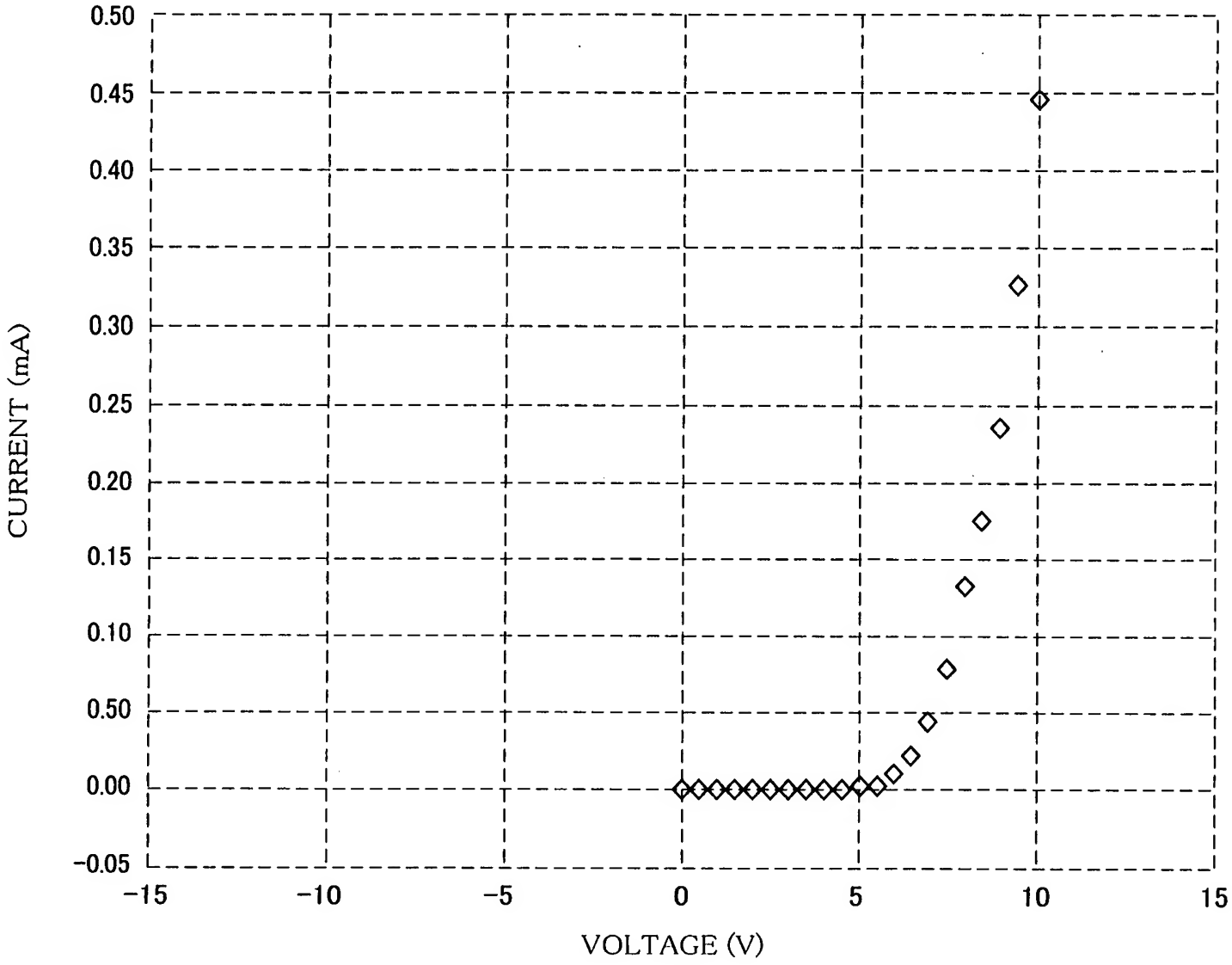

FIG. 9 (a)

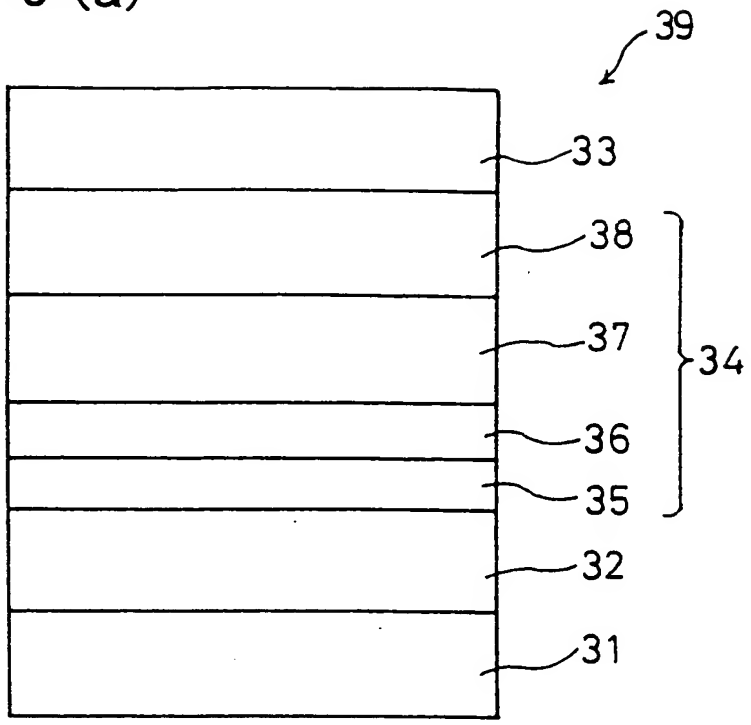

FIG. 9 (b)

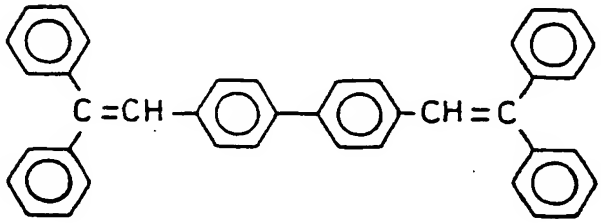

FIG. 10

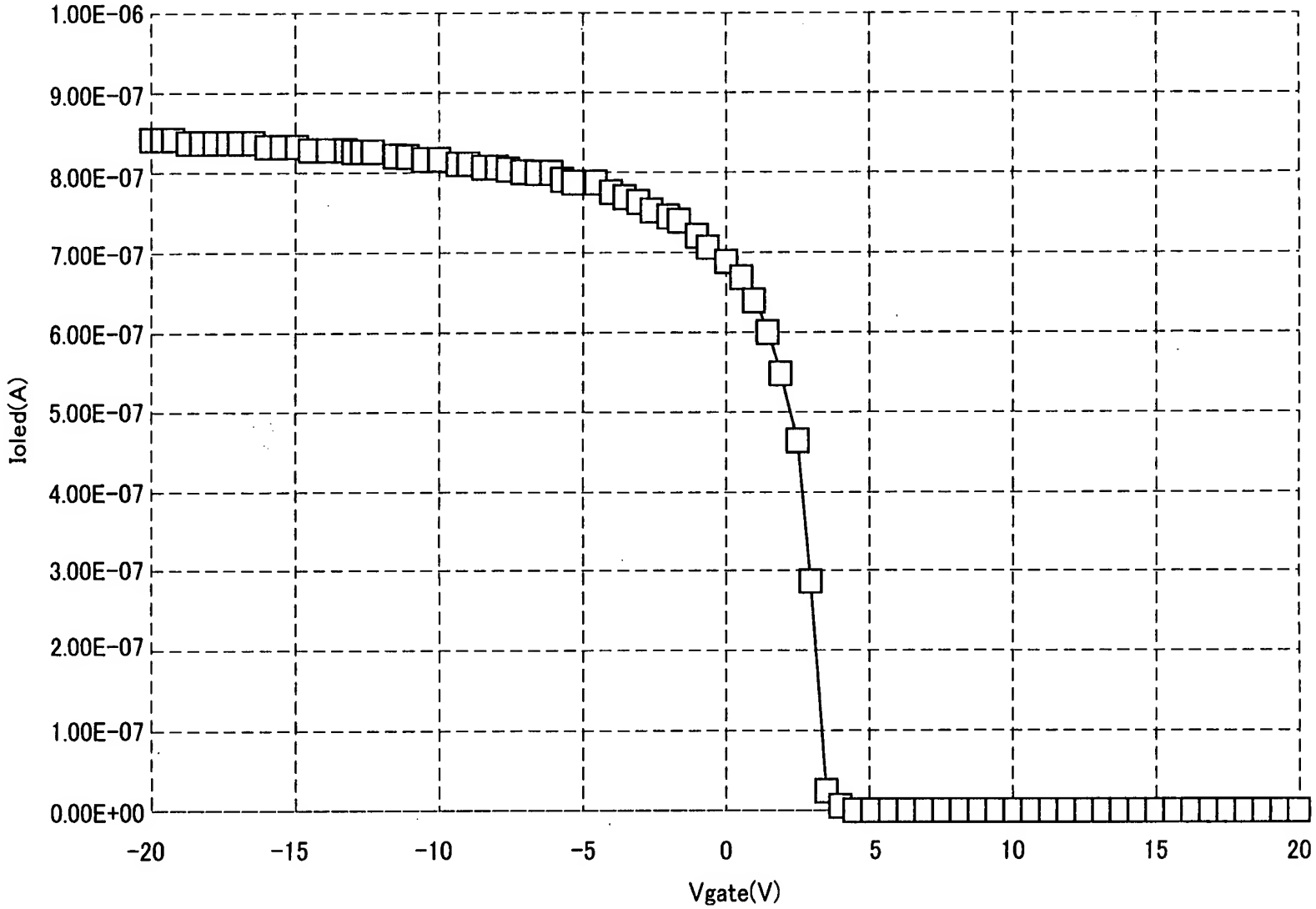

FIG. 11

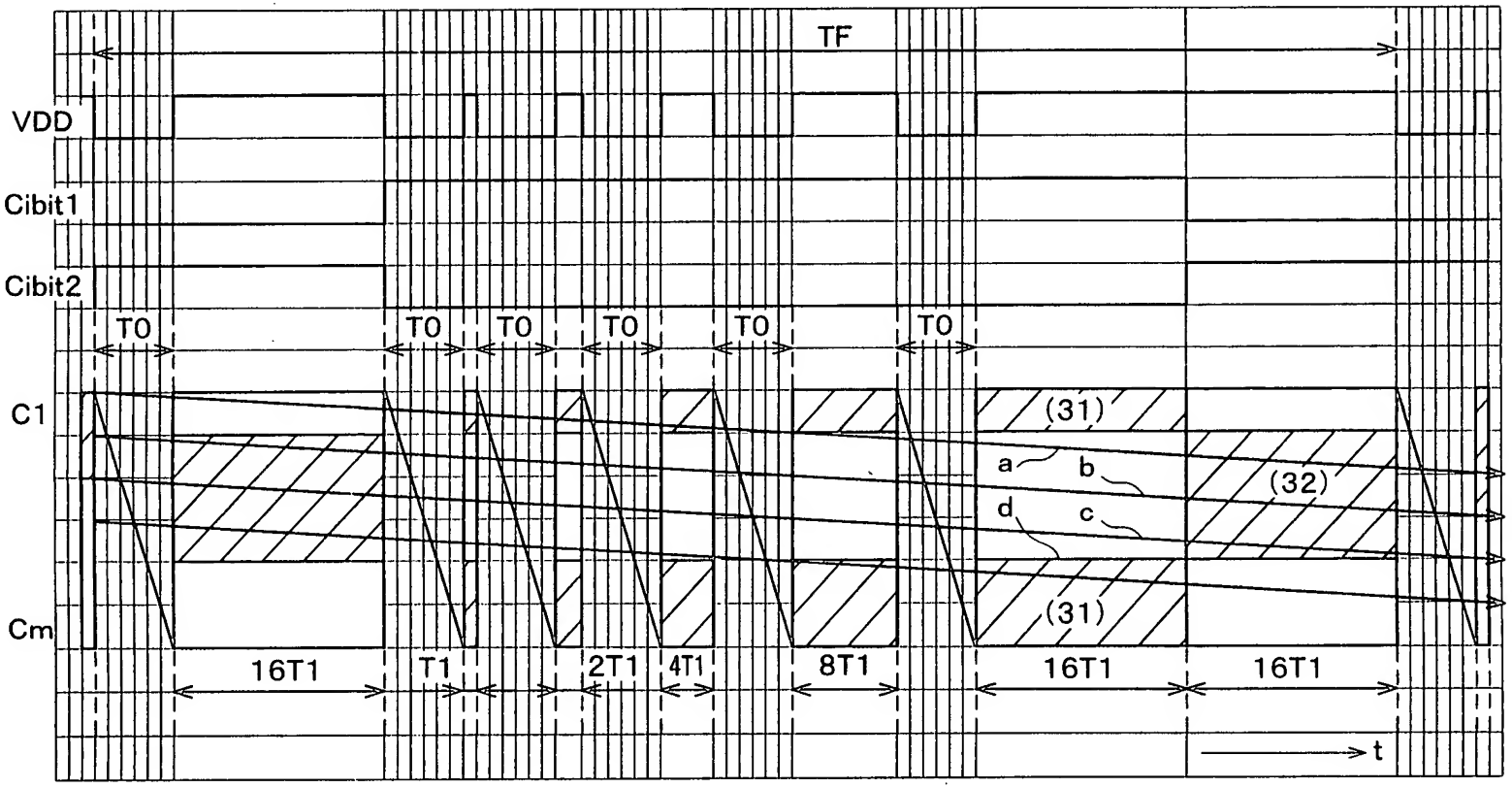

FIG. 12

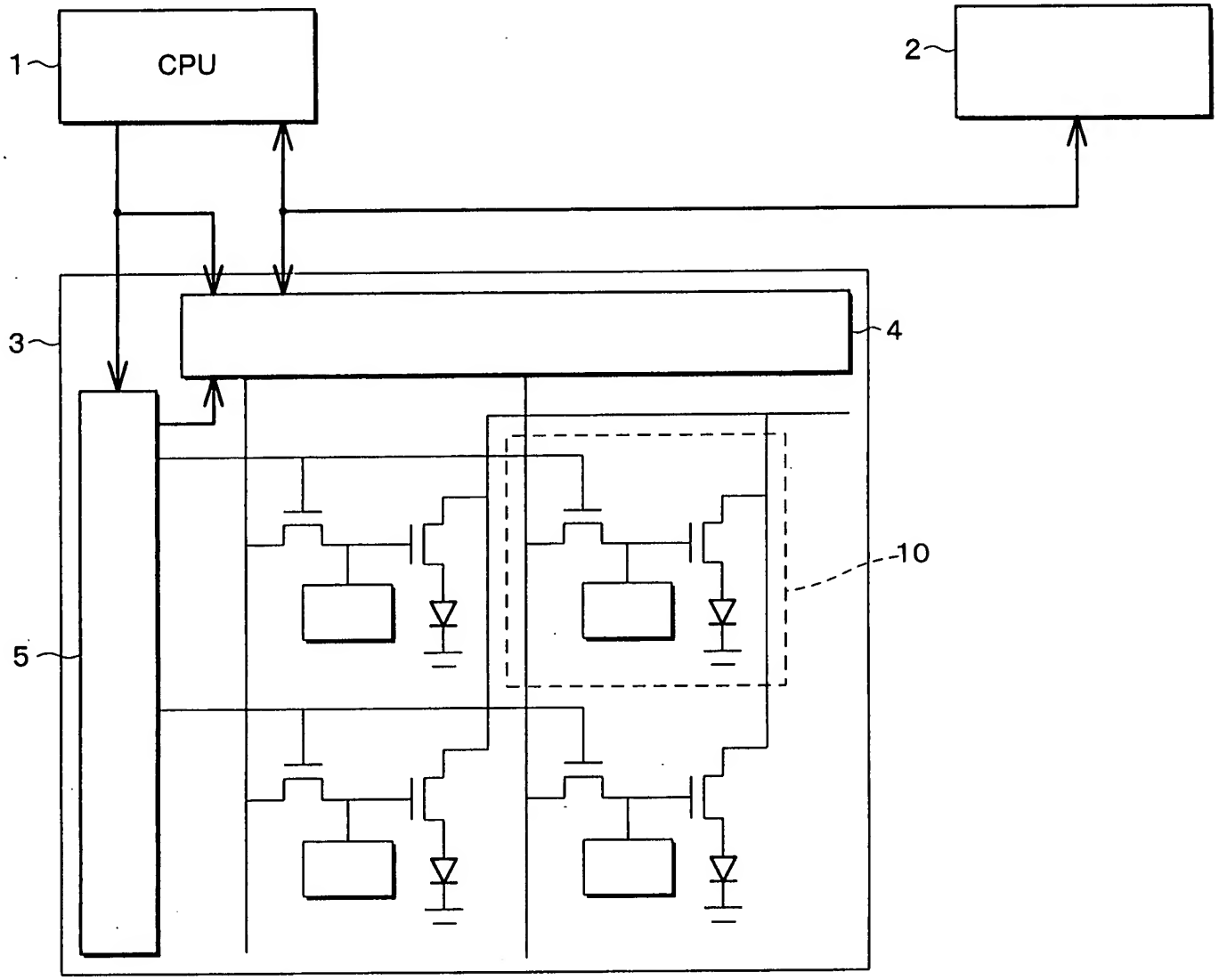

FIG. 13

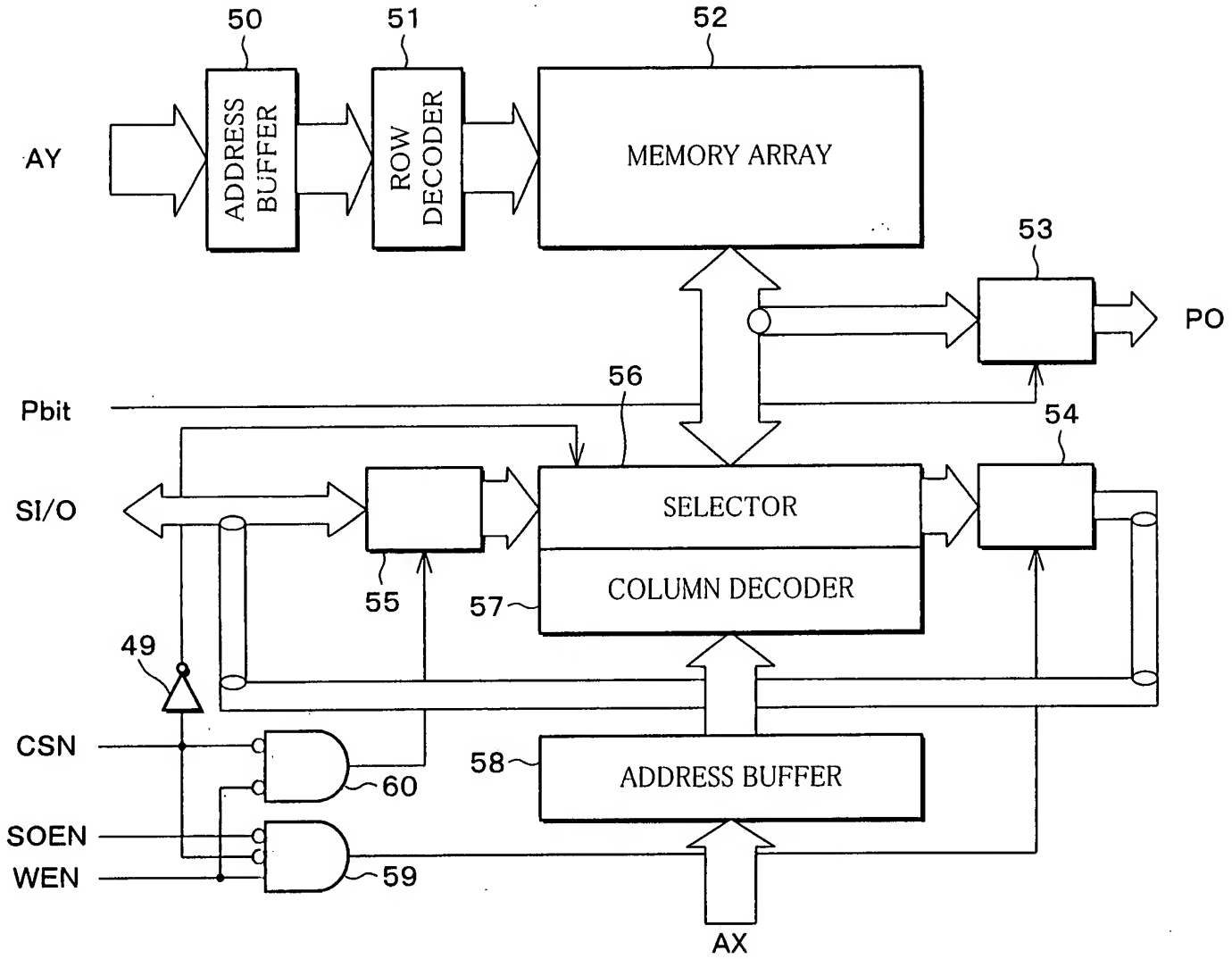

FIG. 14

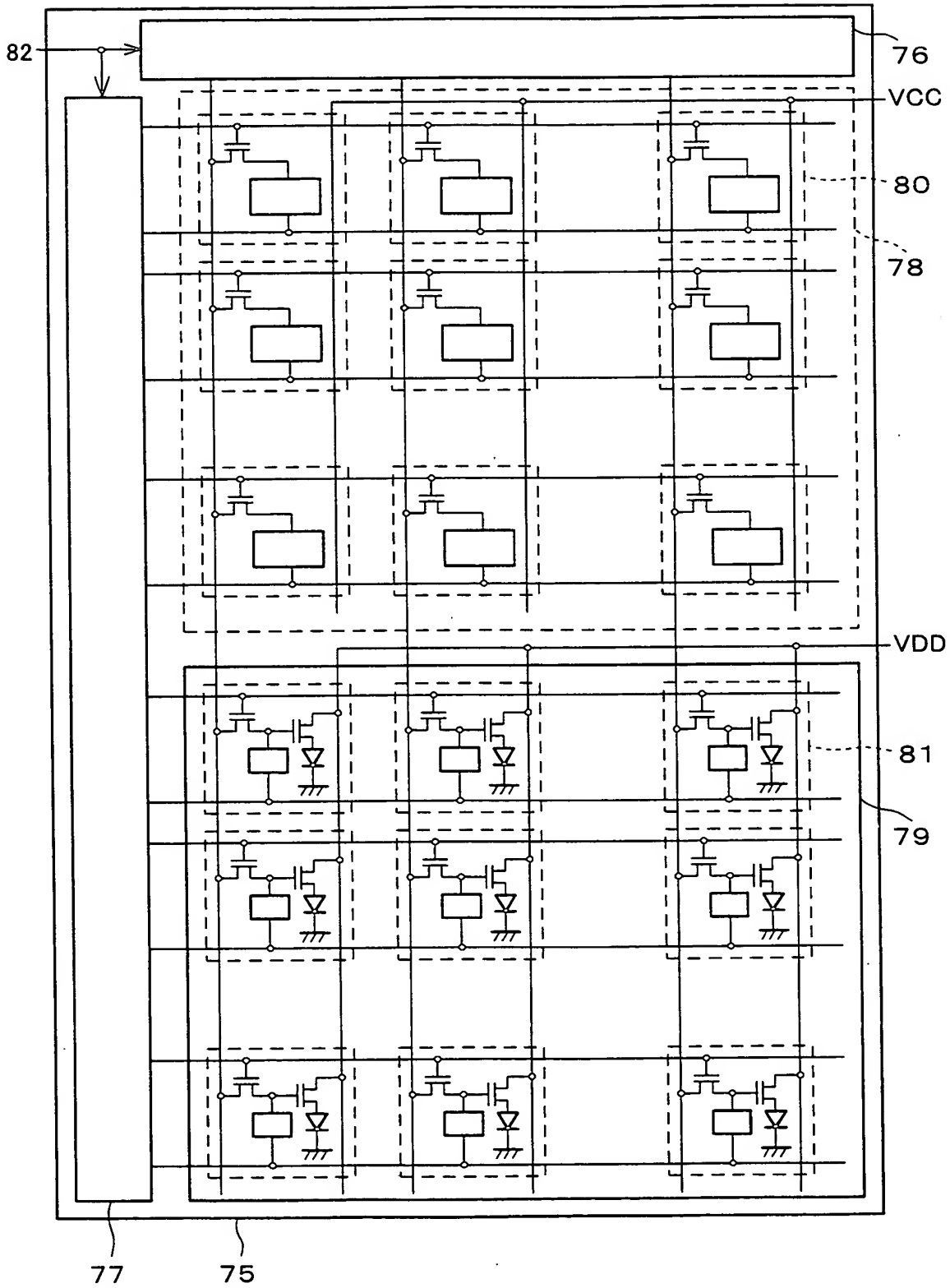

FIG. 15

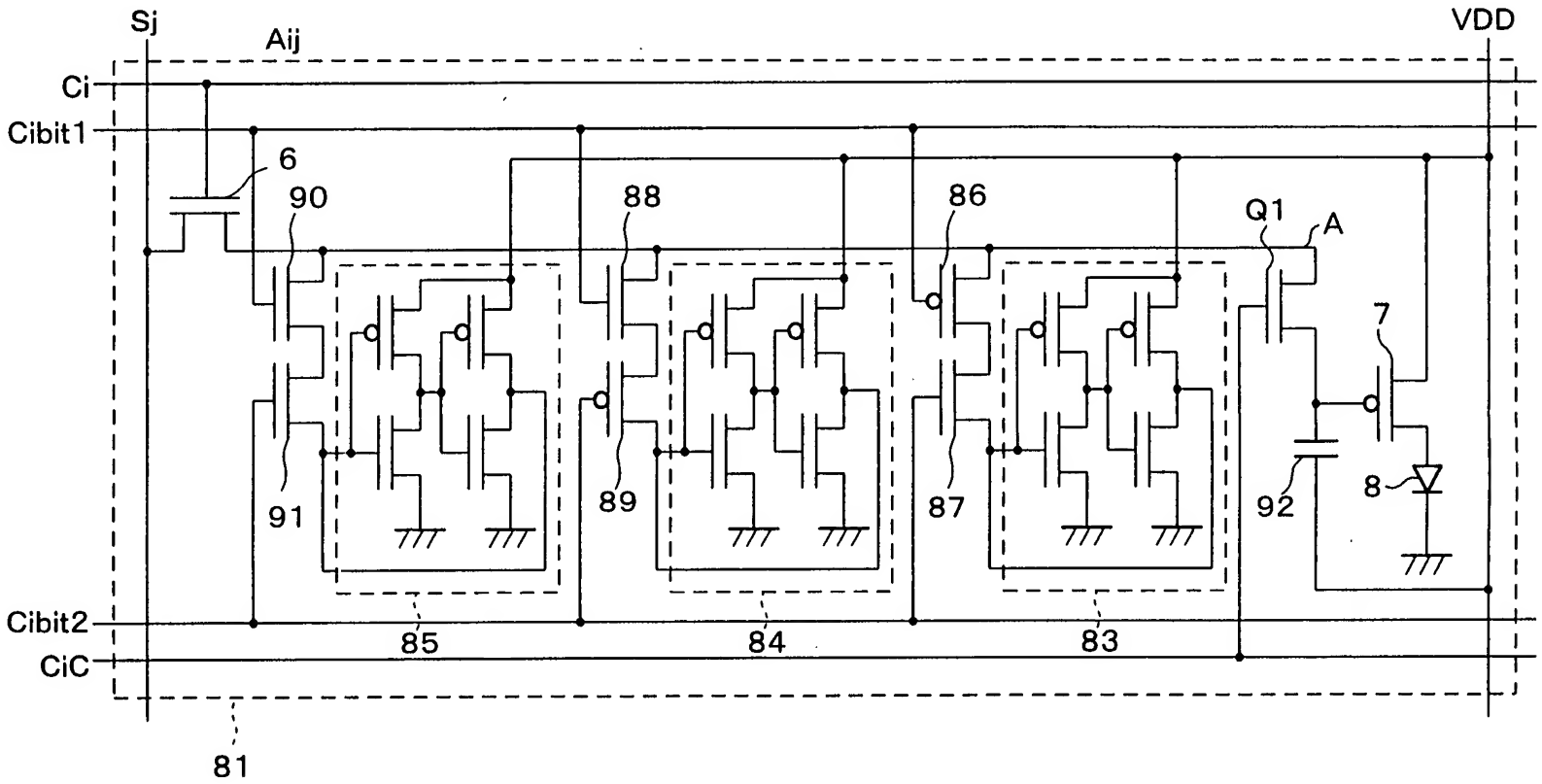

FIG. 16

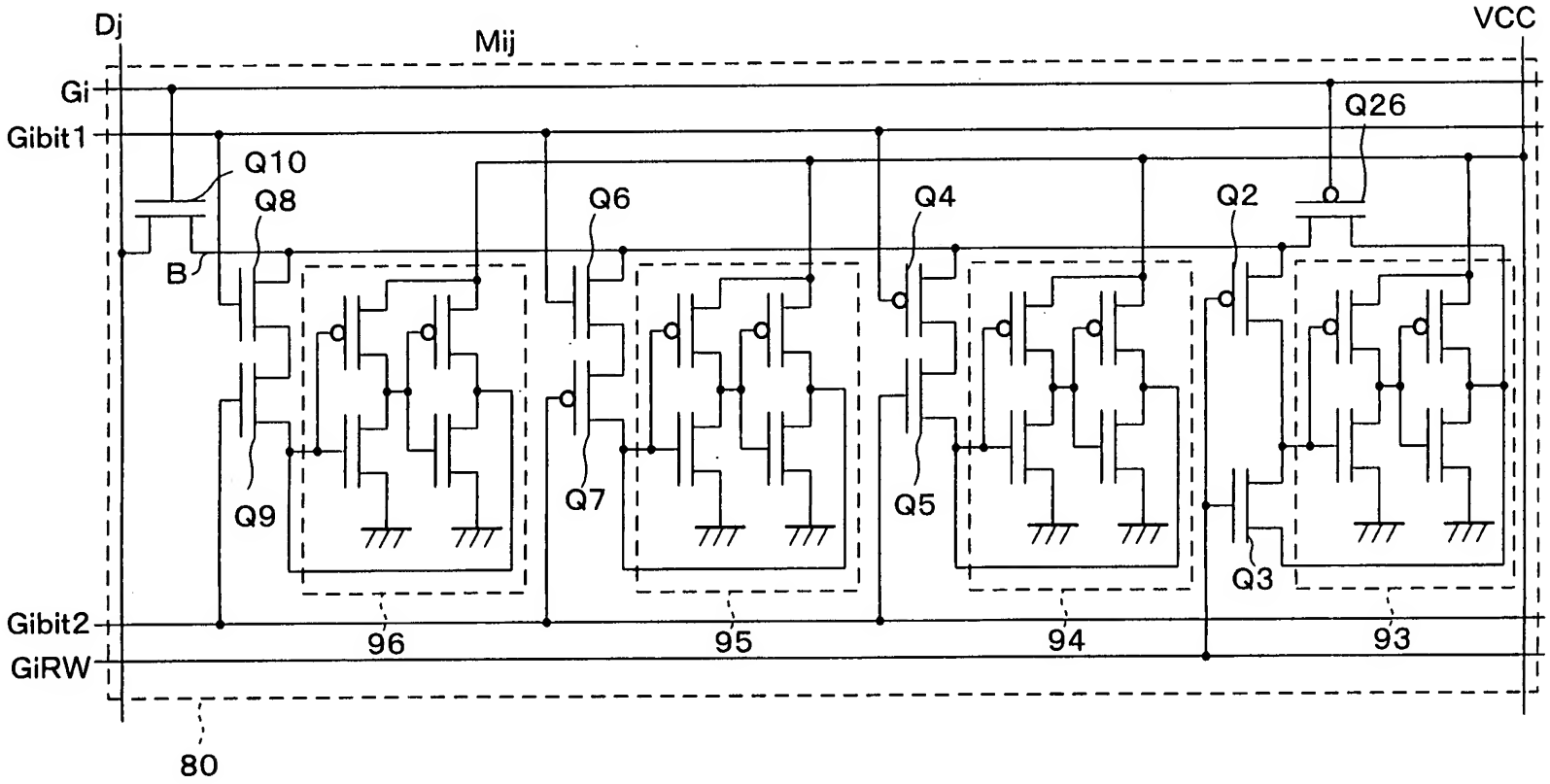

FIG. 17

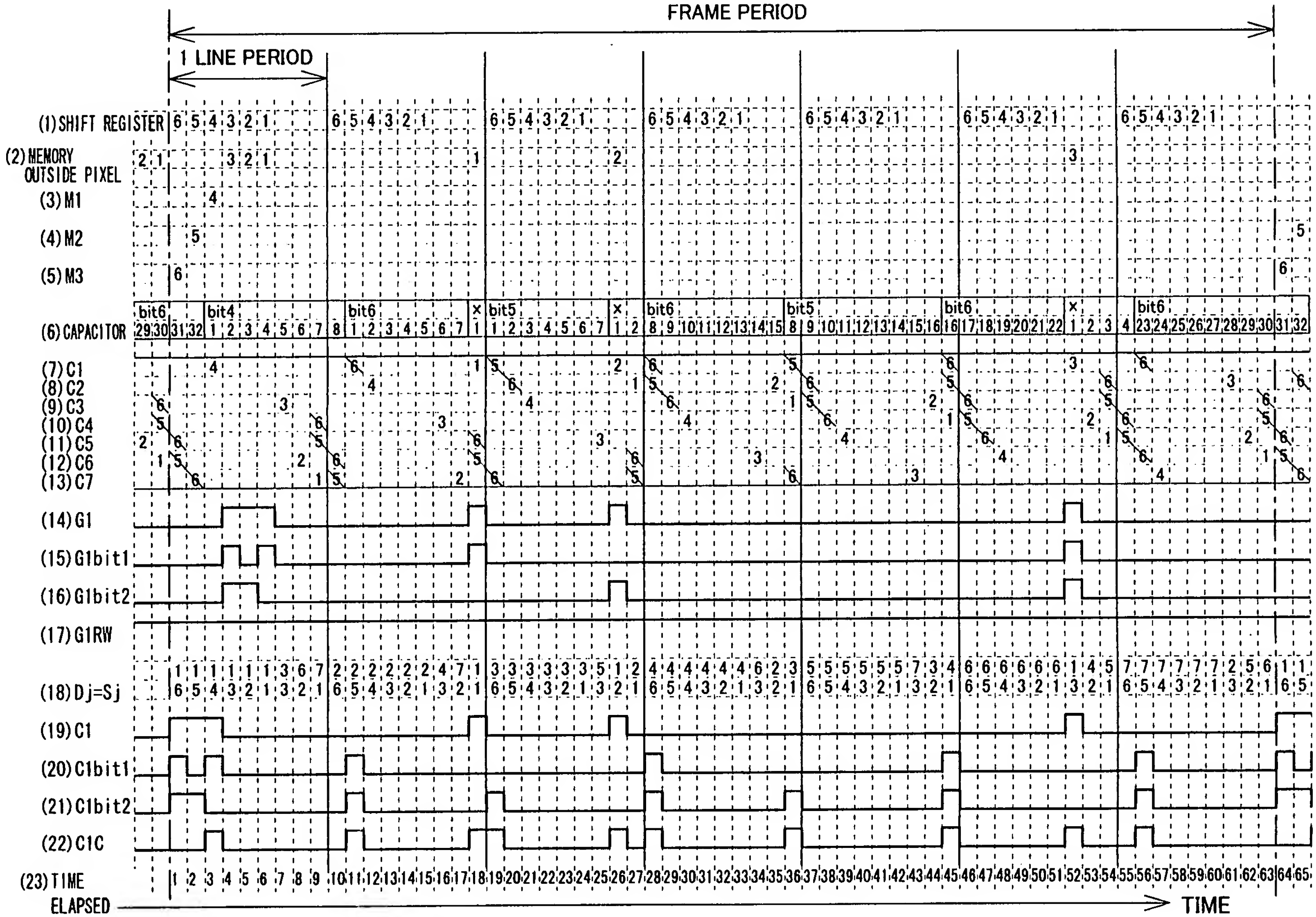
FRAME PERIOD
1 LINE PERIOD
(1) SHIFT REGISTER
(2) MEMORY OUTSIDE PIXEL
(3) M1
(4) M2
(5) M3
(6) CAPACITOR
(7) C1
(8) C2
(9) C3
(10) C4
(11) C5
(12) C6
(13) C7
(14) G1
(15) G1bit1
(16) G1bit2
(17) G1RW
(18) Dj=Sj
(19) C1
(20) C1bit1
(21) C1bit2
(22) C1C
(23) TIME ELAPSED
TIME

FIG. 18

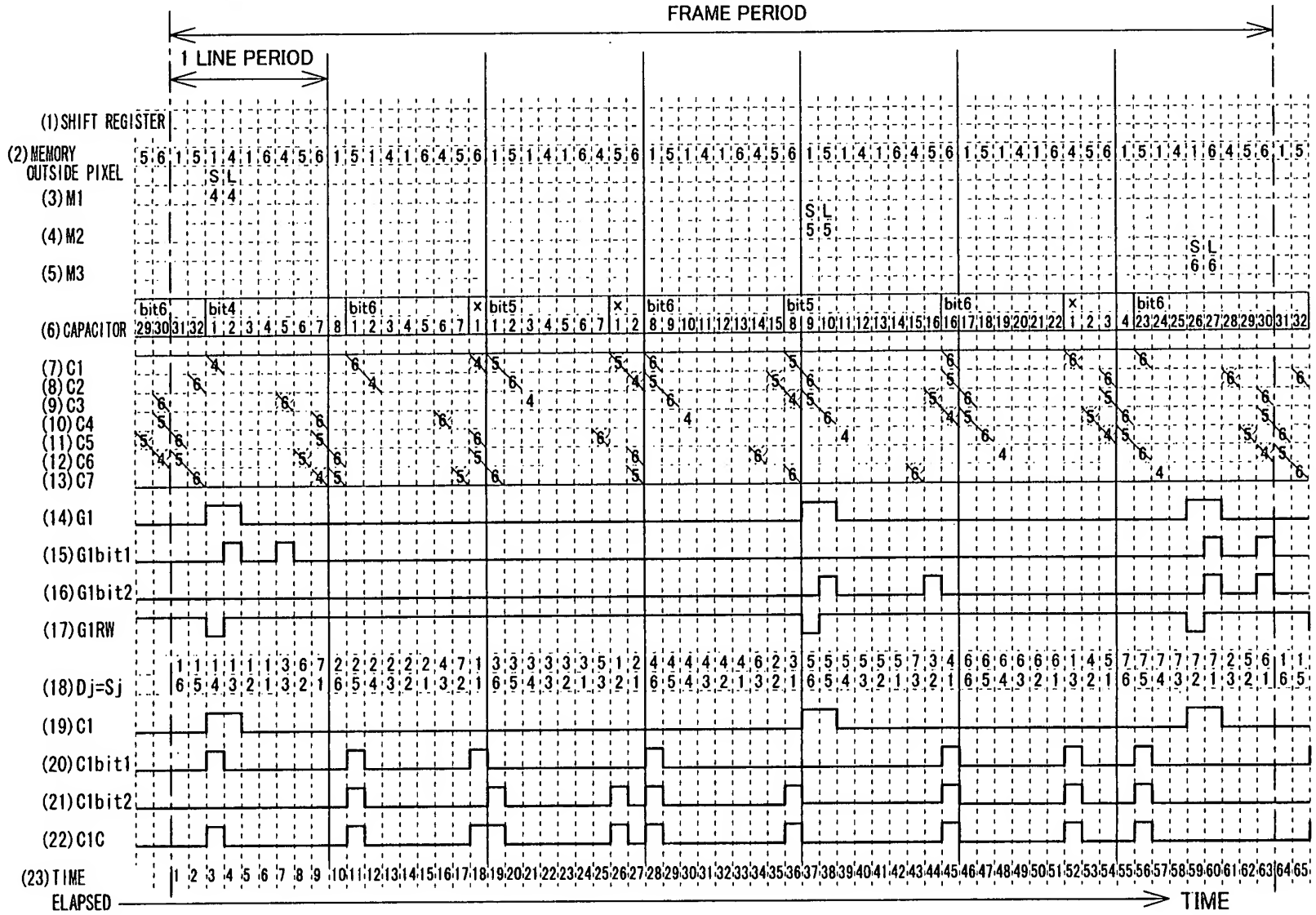

FIG. 19

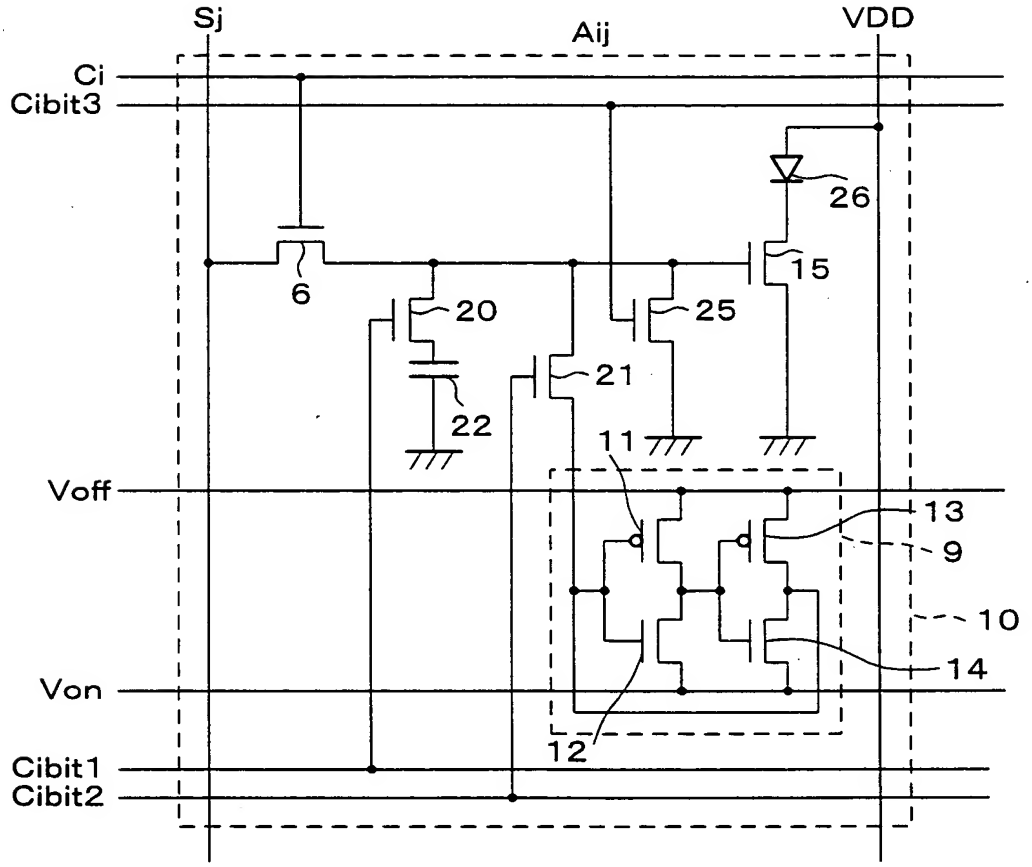
Sj
Aij
VDD
Ci
Cibit3
26
6
15
20
25
21
22
11
Voff
13
9
10
14
Von
12
Cibit1
Cibit2

FIG. 20

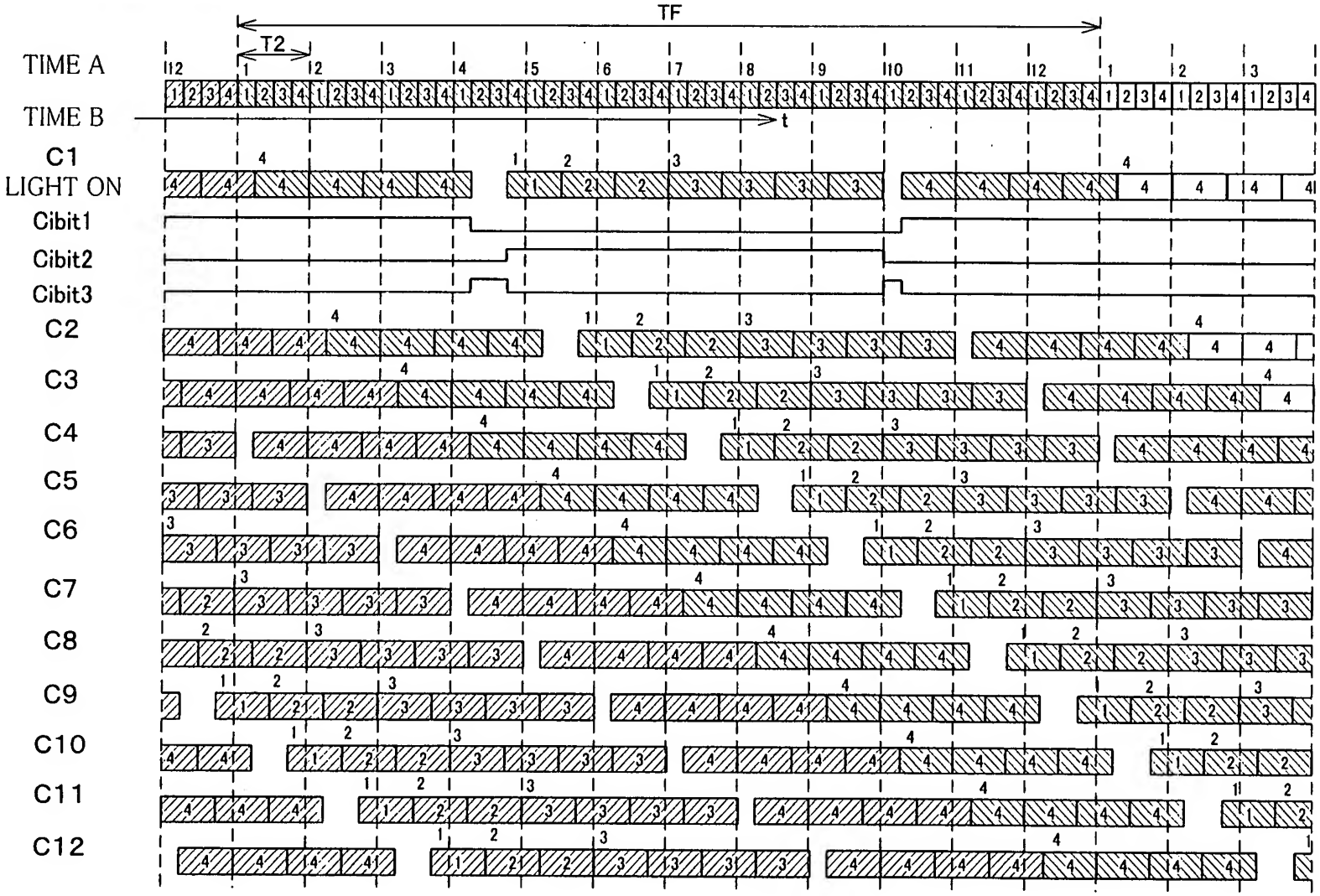

FIG. 21

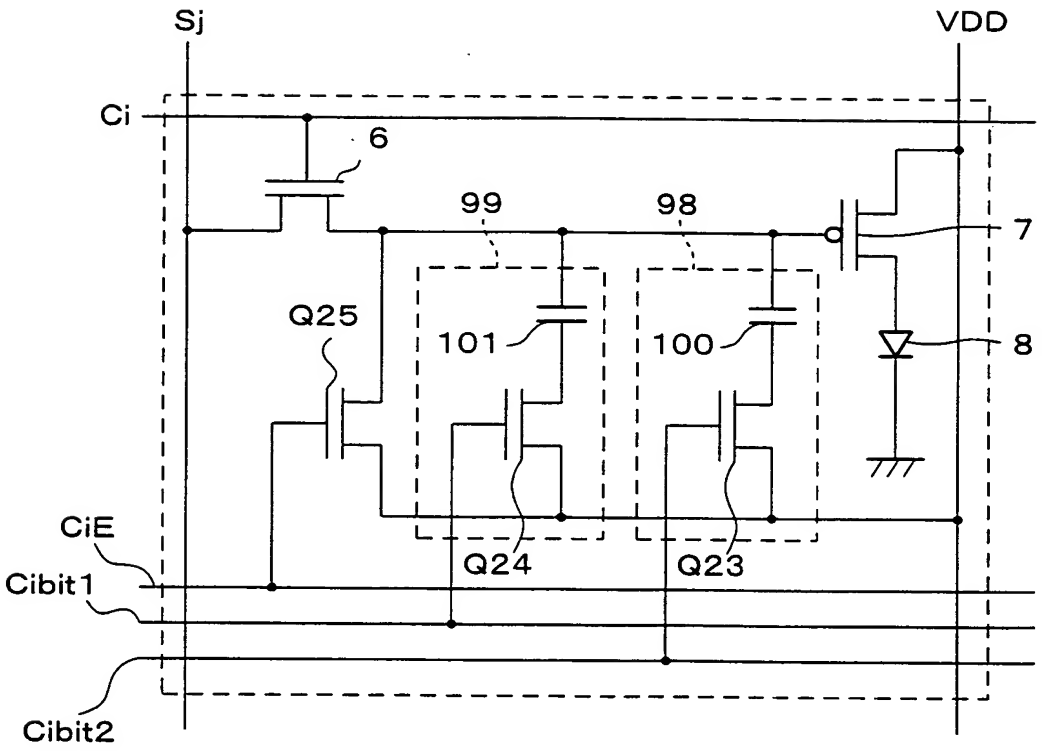

FIG. 22

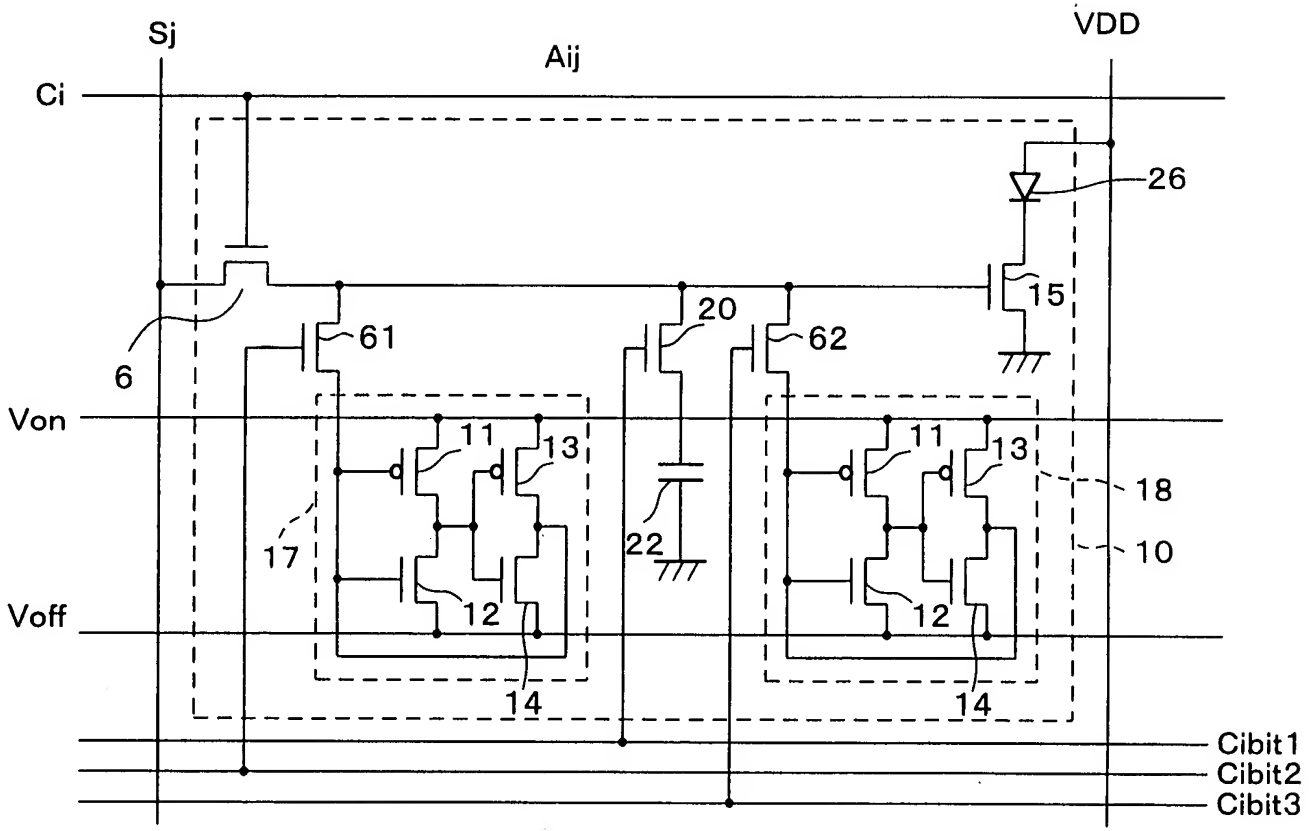

FIG. 23

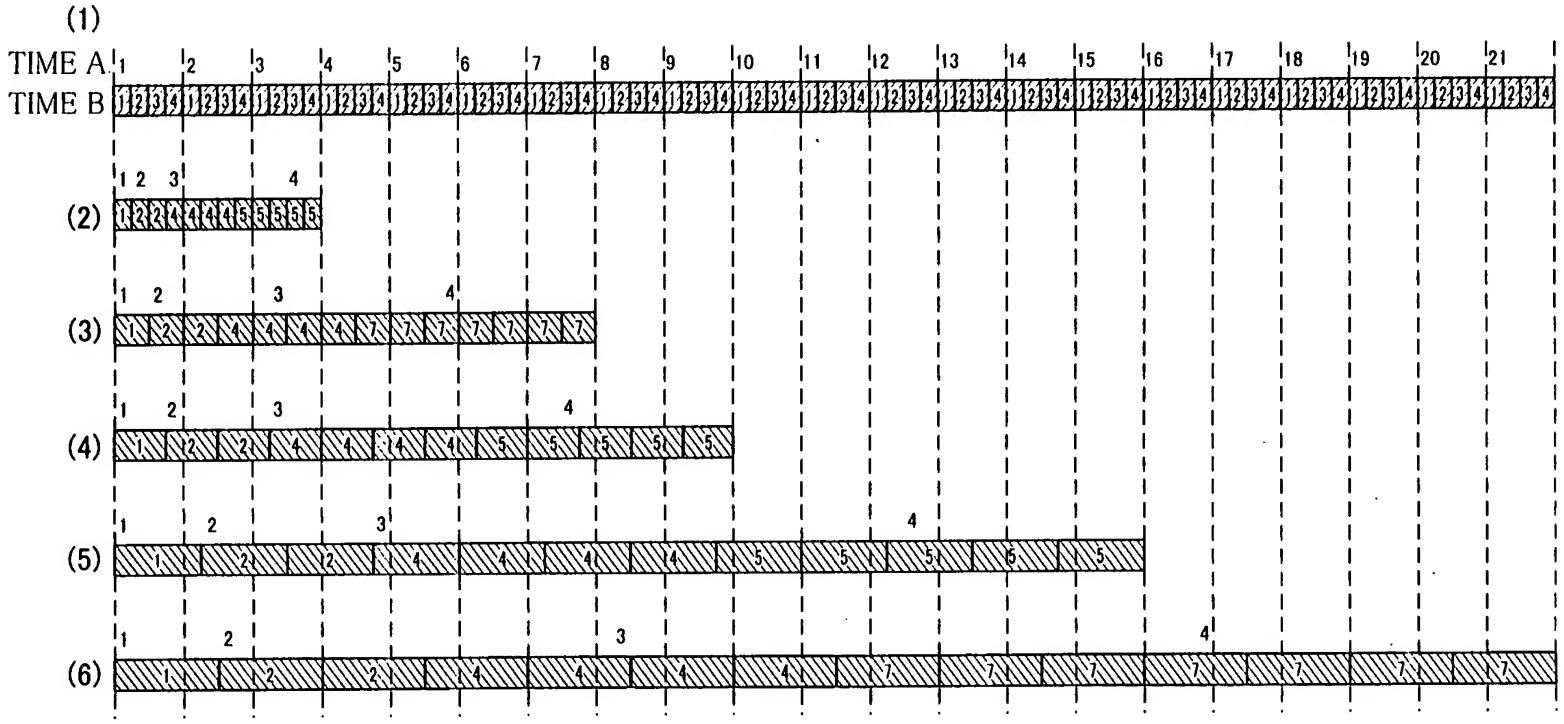

FIG. 24

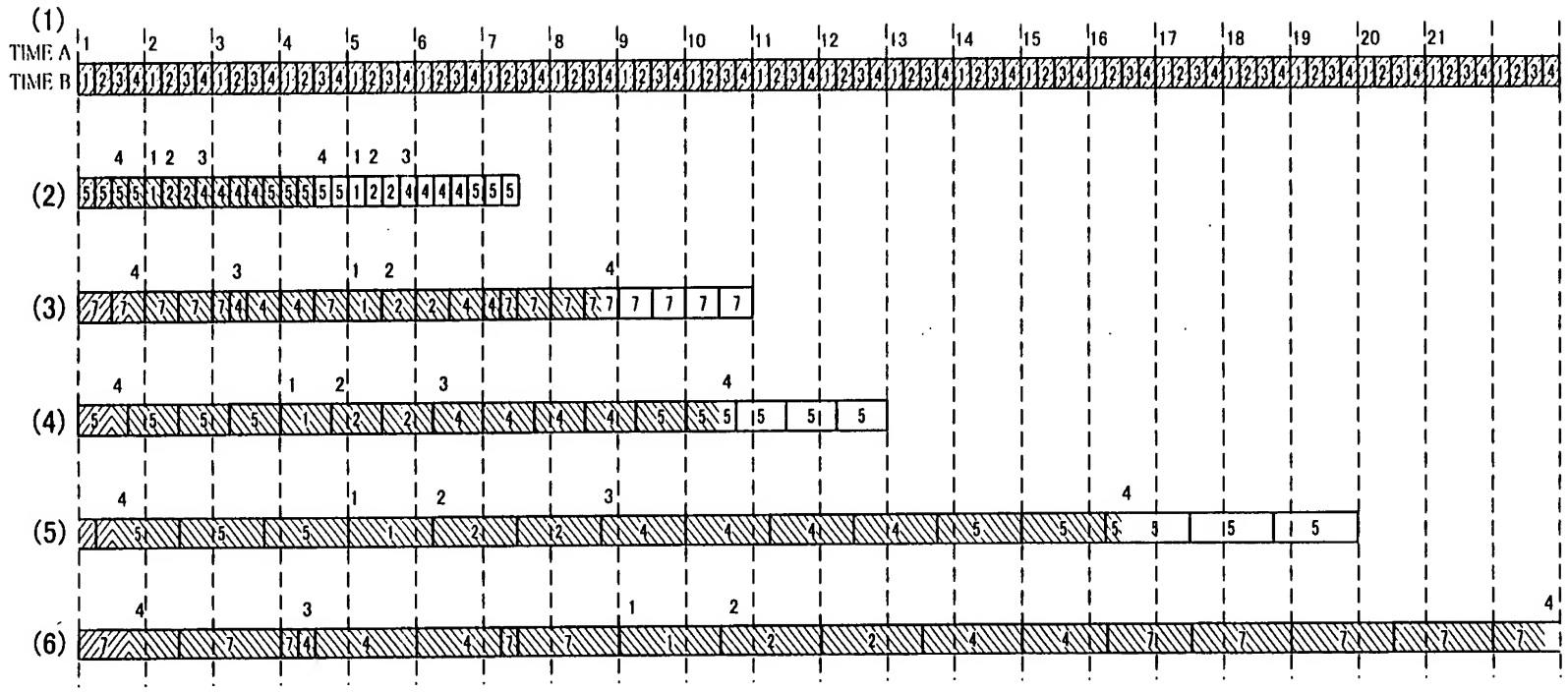

FIG. 25

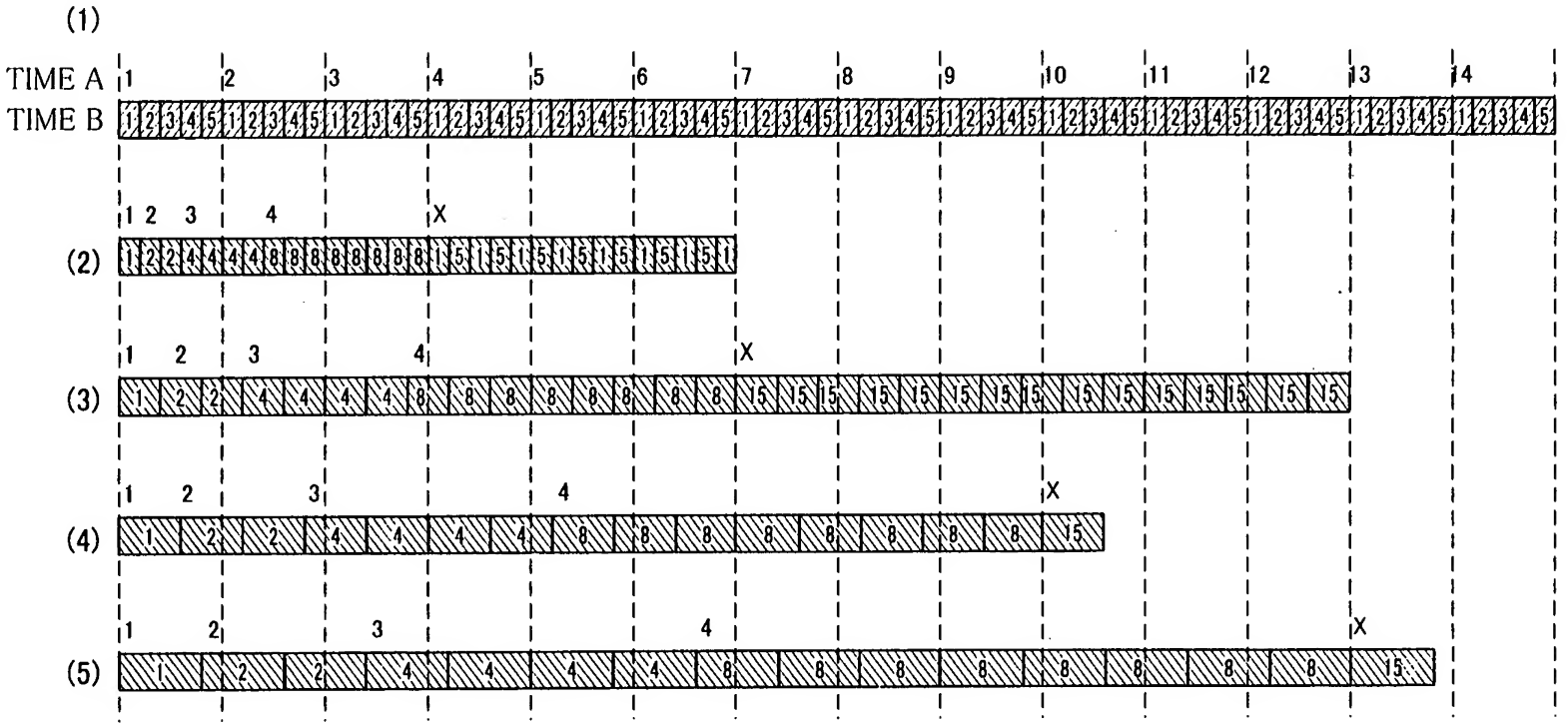

FIG. 26

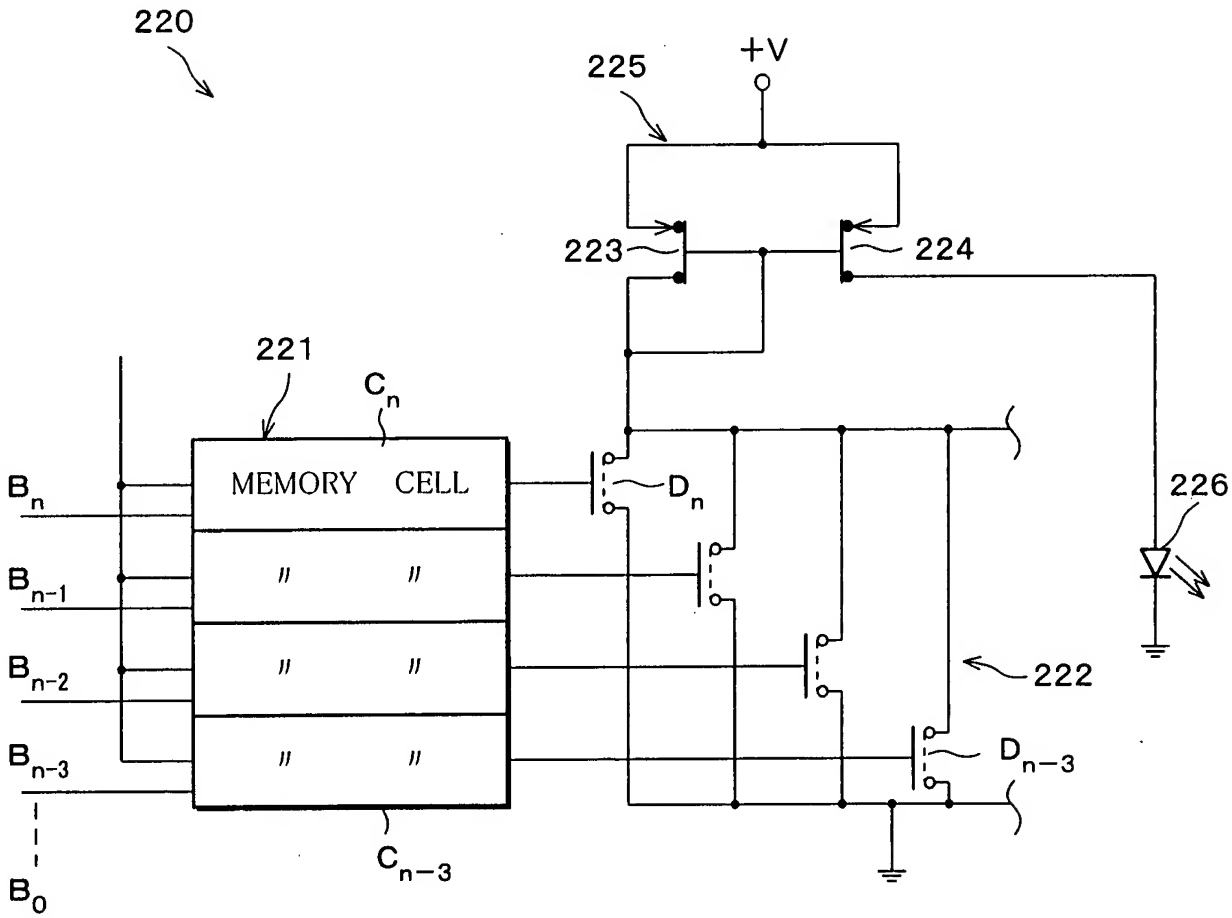

FIG. 27

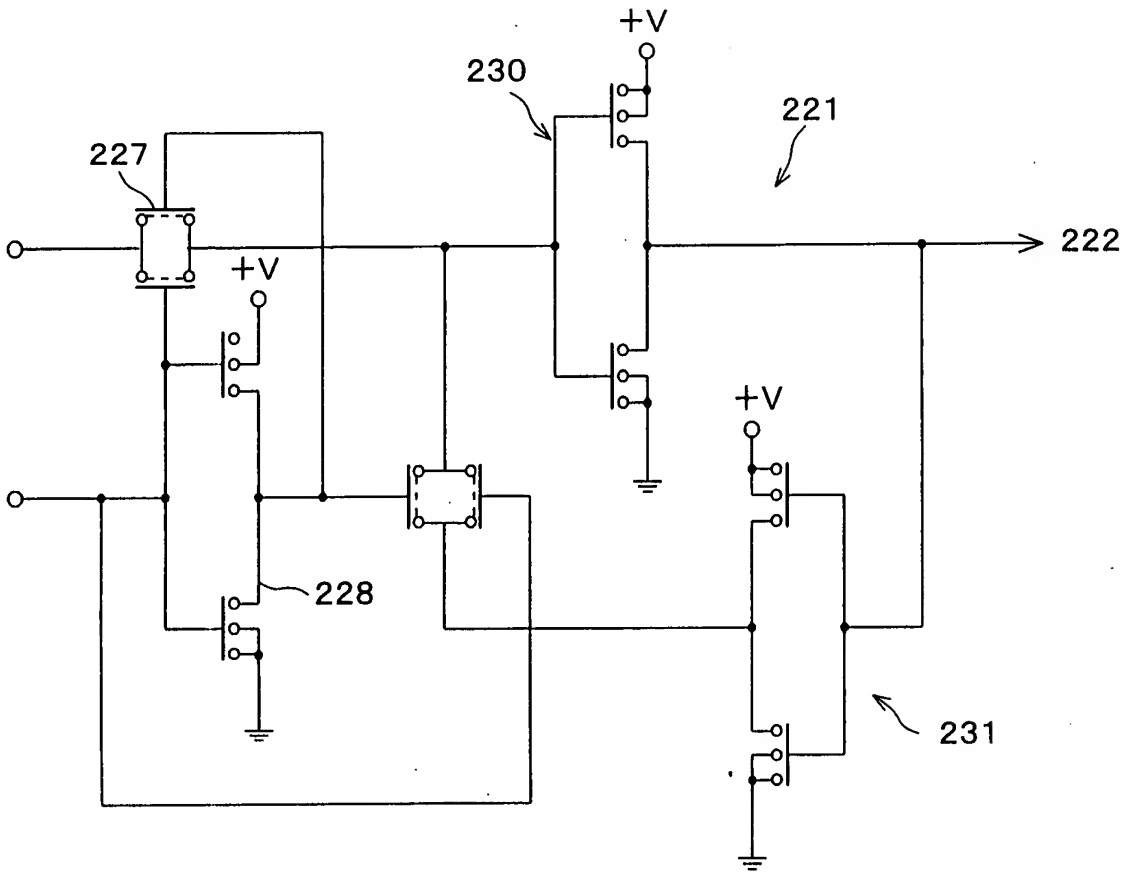

FIG. 28

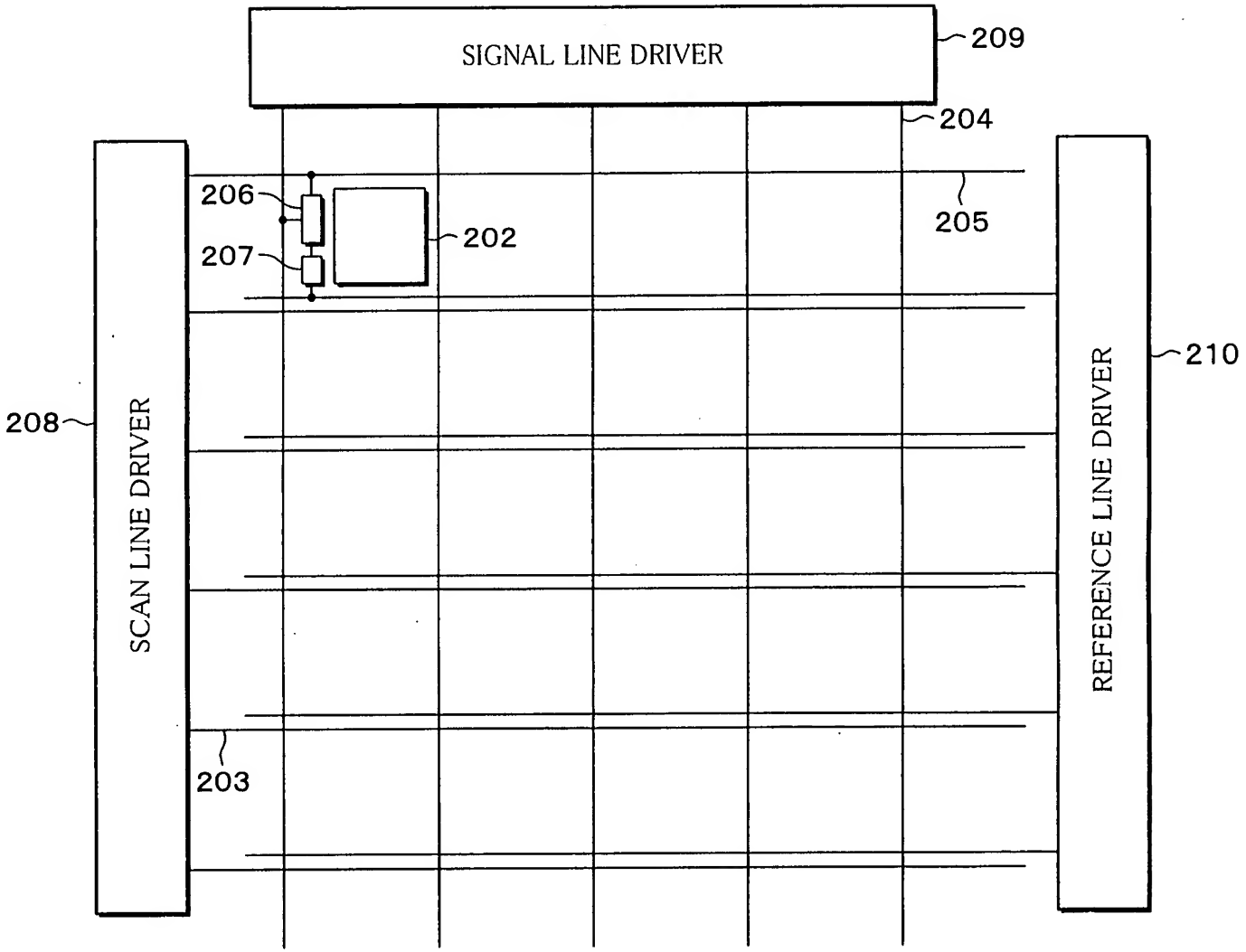

FIG. 29

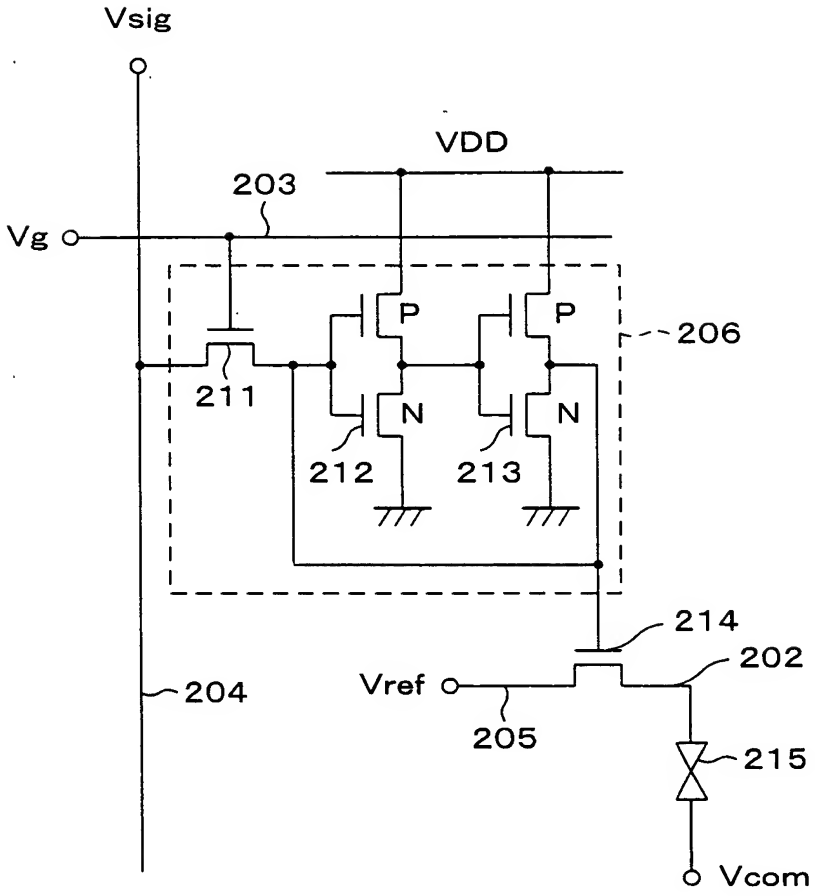
Vsig
VDD
203
Vg
P
P
206
211
N
N
212
213
214
202
204
Vref
205
215
Vcom

FIG. 30

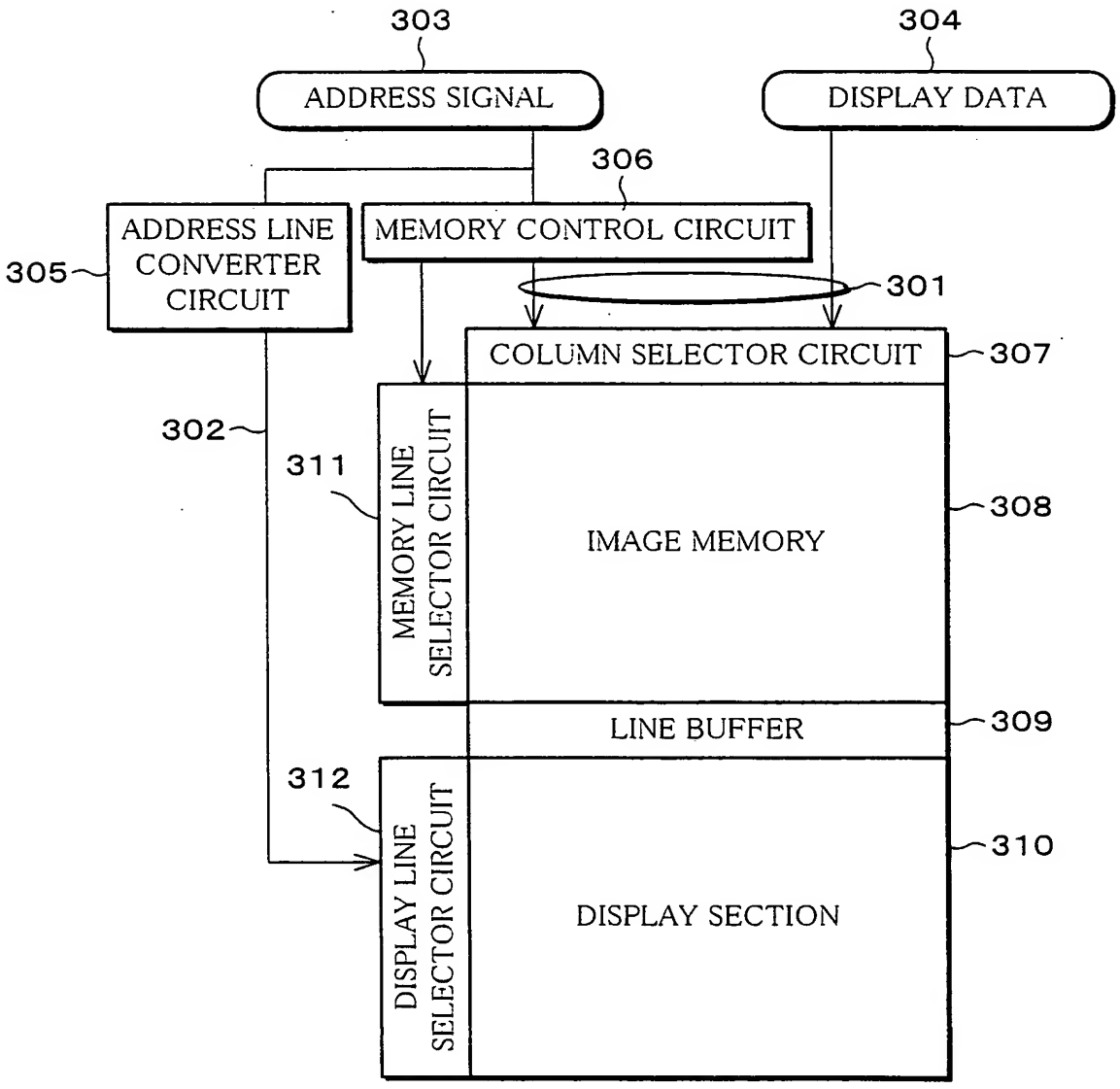
303
304
ADDRESS SIGNAL
DISPLAY DATA
306
ADDRESS LINE CONVERTER CIRCUIT
MEMORY CONTROL CIRCUIT
305
301
COLUMN SELECTOR CIRCUIT
307
302
311
MEMORY LINE SELECTOR CIRCUIT
IMAGE MEMORY
308
LINE BUFFER
309
312
DISPLAY LINE SELECTOR CIRCUIT
DISPLAY SECTION
310

FIG. 31

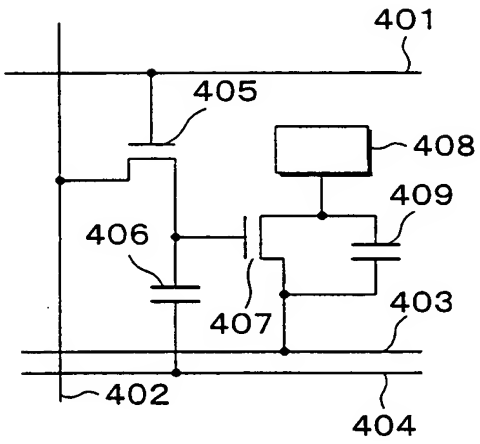
401
405
408
409
406
407
403
402
404

FIG. 32

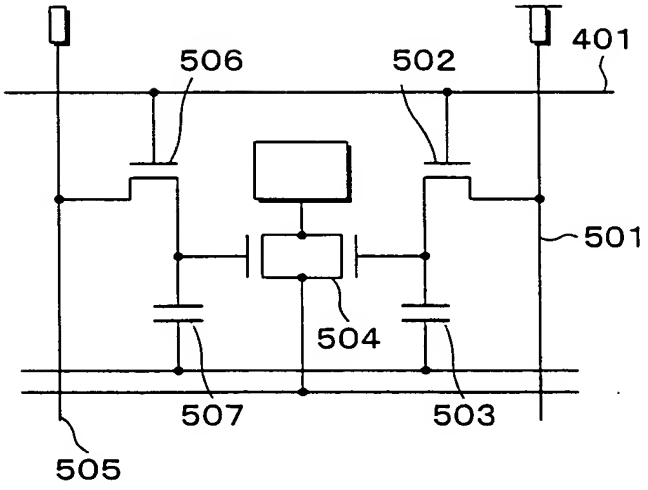
506
502
401
501
504
507
503
505

FIG. 33

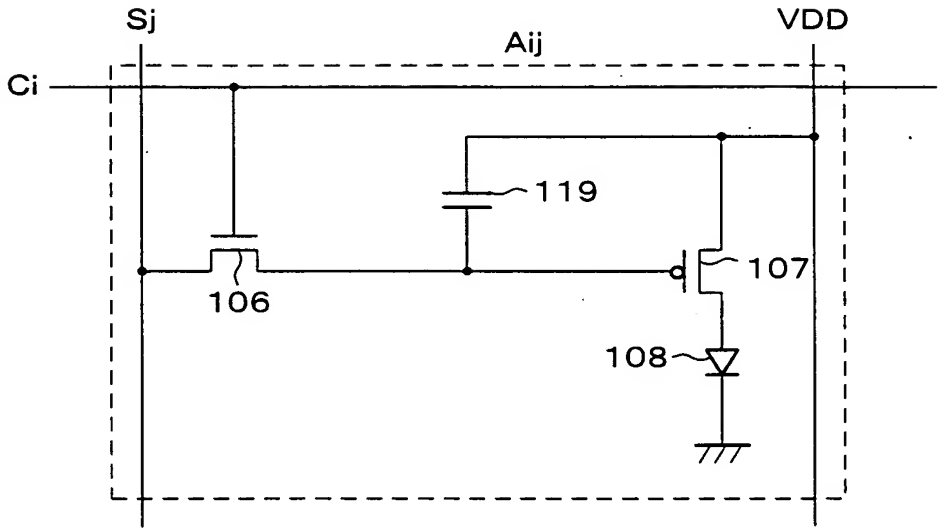

FIG. 34

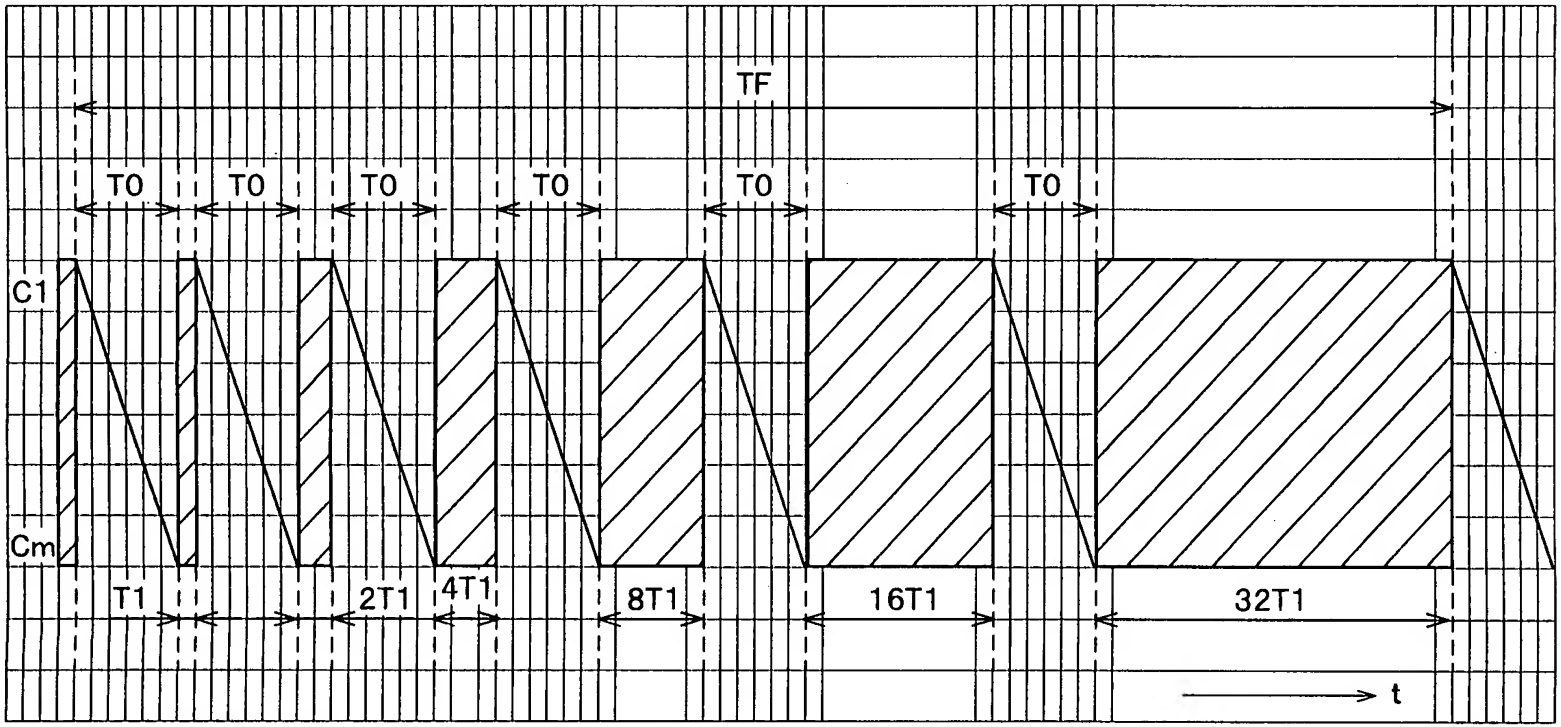

FIG. 35